

eWLB

Embedded Wafer Level Ball Grid Array

We offer customers a high performance fan-out wafer level packaging (FOWLP) solution that provides significant bandwidth, performance, form factor and cost benefits compared to other packaging technologies available today.

Proven Leadership

- Versatile platform for advanced system level integration
- Highest integration density commercially available in the industry today
- Flexibility to integrate die from diverse processes, manufacturing sources & silicon wafer nodes for increased functionality
- Excellent mechanical, electrical & thermal performance
- Effectively accommodates new lithography nodes
- Flexible, cost effective 2D, 2.5D & 3D solutions across a broad range of market segments & applications

Features

Performance

- Unprecedented flexibility in 2.5D & 3D integration with Si partitioning capabilities
- Advanced dielectric materials for highly reliable, power-efficient solutions
- Strong electrical performance (capable to beyond 80GHz) and fit for mmWave/5G devices
- Highly effective heat dissipation for strong thermal performance
- KGD process helps achieve strong yields (99.9%)

Form Factor

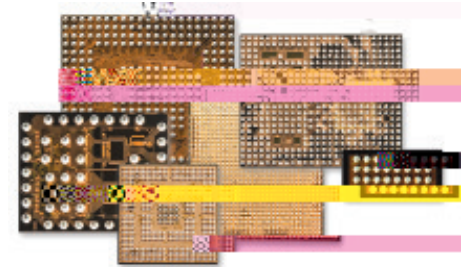
- Maximum I/O density; 1.5-2X increase in routing density in the smallest, thinnest footprint commercially available today
- Thin film processing enables very fine lines for X,Y routing (line and width spacing down to 2µm/2µm), very fine via pitches & thin dielectrics
- Die-to-die, die-to-passives, & passives-to-passives placement distances below 100µm
- Fine pitch copper (Cu) pillar bumps provide tighter pitch for 2.5D/3D designs
- Industry's thinnest 3D PoP solutions (ultra thin z-height of 0.3mm with stacked thickness down to 0.8mm height)

Cost

- Well established, high volume manufacturing process enables scaling devices to larger panel sizes for cost reduction
- Thin film interconnection offers lowest cost structure over competing advanced manufacturing approaches
- Elimination of substrate results in a thinner package with lower warpage, simplifies supply chain & reduces costs
- 2.5D and 3D options offers a more cost effective & infrastructure-friendly alternative to expensive TSV integration

Market Leader in FOWLP Technology

Embedded Wafer Level Ball Grid Array (eWLB) is a versatile fan-out wafer level packaging platform (FOWLP) designed to address the growing mismatch in interconnect gap, higher levels of integration, improved electrical performance and shorter vertical interconnects. The eWLB platform provides a more space-efficient package design enabling a smaller footprint, higher density input/output (IO) and lower package profiles.

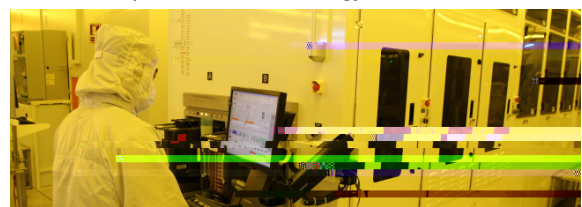


Assembled directly on a silicon wafer, this chip-first, face-down FOWLP approach is unconstrained by die size, providing the design flexibility to accommodate an unlimited number of interconnects between the package and the application board for maximum connection density, finer line/spacing, improved electrical and thermal performance and small package dimensions to meet the relentless form factor requirements and performance demands of the mobile market.

eWLB's flexible manufacturing process can reduce substrate complexity and costs while achieving very dense interconnection in a range of reliable, low-warpage 2D, 2.5D and 3D solutions including small die, large die, stacked or side-by-side multi-die and ultra-thin options across a broad range of market segments and applications.

The basic structure of eWLB, thin film processing, has enabled us to create eWLB-based interposers that can connect one active die to another, enabling very dense interconnection with more effective heat dissipation, improved processing speed and the flexibility to integrate die from different manufacturing sources. The result is a proven 2.5D solution that is superior to Through Silicon Via (TSV) in terms of overall cost effectiveness and process simplicity.

Our 3D System-in-Package (SiP) and Package-on-Package (PoP) solutions include embedded multiple passives and active components, face-to-back or face-to-face options, and single-sided, 1.5-sided and double-sided ultra-thin PoP configurations. For applications requiring full 3D integration, our face-to-face eWLB PoP configuration provides a direct vertical interconnection between an application processor die and a memory die through the eWLB mold layer to enable a high bandwidth, very fine pitch structure with performance that parallels TSV technology.



Application Space

When determining the optimal platform among the space of device